REMARKS

Reconsideration of the application is respectfully requested.

Claims 1 and 16 stand rejected as being anticipated by U.S. Patent No. 6,370,661 issued to Miner ("Miner"). With respect to claim 1, the rejection is overcome as Miner does not teach or suggest a system having a first random access memory, a memory testing engine to execute test operations on the memory, a memory controller for accessing the memory, a bus controller, a processor, and a bus that connects the processor to the bus controller. The bus controller is to provide the processor access to the memory via the memory controller. In addition, the processor is to control the memory testing engine via the bus and the controller, where the testing engine using data address and control pathways that are used by the bus controller so that if data traffic is being passed to a memory module by the bus controller, the memory testing engine cannot run a test function.

In Miner, an apparatus for testing memory in a microprocessor is shown, where the microprocessor has test management logic and test execution logic located within. The execution logic 560 directly interfaces with the memory 510 via a bus 532, 564. Management logic 570 interfaces to test execution logic 560 via a bus 574. [Miner, col. 10, lines 5-15] There is no teaching or suggestion to modify Miner so as to arrive at the system of Applicants' claim 1 as amended here, because the techniques in Miner are primarily employed to test memories in a microprocessor by a test controller 580, and not to a system in which the random access memory is coupled with an application specific integrated circuit. Accordingly, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

As to claim 16, this claim has been amended to recite a method that is not taught or suggested by Miner. In Miner, a test controller sends test parameters to test management logic that is within a microprocessor, and test execution logic 560 tests the microprocessor's own memory. This does not teach or suggest a method where memory is accessed via multiple bus controllers, respectively, a plurality of random access memories are tested using memory testing engines, respectively, accessing from the processor the random access memories via the bus controllers, respectively, and

accessing from the bus controller the random access memories using a number of memory controllers, respectively.

In Miner, a single processor with multiple memories 510 is tested by an external test controller 580 which provides parameters to management logic 570, and it is test execution logic 560 that sends test comparisons on data obtained from read from memory. There is no teaching or suggestion that multiple memory controllers be provided in Miner such that a method according to claim 16 as amended here, could be practiced. Reconsideration and withdrawal of the rejection of claim 16 is therefore respectfully requested.

Turning now to claim 30, this claim is not anticipated or obvious in view of Miner, for at least the reasons given in Applicants' amendment and response that was filed October 2004, at page 9, last full paragraph. In the current Office Action, at page 4, the Examiner asserts that Miner teaches an apparatus 500 for testing memory circuits 510 in a microprocessor 501 (testing memories within an ASIC). The Applicants respectfully disagree with this interpretation of Miner, because testing of a microprocessor, which includes built-in self-test circuitry and memory, does not teach or suggest accessing a memory associated with an ASIC via a bus controller, and configuring a memory test engine by writing to the controller over the bus, and processing a signal from the memory test engine that a test of that memory is complete.

The Examiner's attention is directed to the attached sheets which are printouts of online dictionaries giving their respective meanings for "ASIC". If one were to adopt either one of these meanings, it would be clear to one of ordinary skill in the art that a test controller 580 testing built-in memories of a microprocessor does not teach or suggest accessing a memory that is associated with an ASIC.

Moreover, the phrase "utility bus controller" is used for a utility bus, which is a bus that is used between integrated packages in a system. The on-chip interface to the bus 575 of the microprocessor 501 in Miner does not teach or suggest a utility bus slave controller.

Turning now to claim 44, as was explained in the amendment and response filed in March 2004, at page 15, last paragraph, this claim is directed to a system where the means for giving the initiation means access to each memory and access to the testing means corresponds to, in the case of Fig. 2, a bus 220 followed by a translator 230, a master bus controller 240, and multiple instances of a bus slave controller 250. In the alternative, in Fig. 4, the means for giving the initiation means access to the memories may be an instance of a data transfer engine (DTE) 420 using in situations where a utility bus system, as shown in Fig. 2, is not used. Miner does not teach or suggest such structural components of a system, and neither does it teach or suggest modifications that would be deemed an equivalent under 35 U.S.C. §112, paragraph six.

Any dependent claims not mentioned above are submitted as being neither anticipated nor obvious, for at least the same reasons given above in support of their base claims.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: April 14, 2005

By _____
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on April 14, 2005.

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Margaux Rodriguez *April 14, 2005*

ASIC

Last modified: Thursday, January 29, 2004

Pronounced *ay-sik*, and short for *Application-Specific Integrated Circuit*, a chip designed for a particular application (as opposed to the integrated circuits that control functions such as RAM in a PC). ASICs are built by connecting existing circuit building blocks in new ways. Since the building blocks already exist in a library, it is much easier to produce a new ASIC than to design a new chip from scratch.

ASICs are commonly used in automotive computers to control the functions of the vehicle and in PDAs.

•E-mail this definition to a colleague•

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silicon

(Webopedia)

ONLINE COMPUTING DICTIONARY

ASIC -->

Application-Specific Integrated Circuit

<hardware> (ASIC) An integrated circuit designed to perform a particular function by defining the interconnection of a set of basic circuit building blocks drawn from a library provided by the circuit manufacturer.

(1995-02-15)

Previous: applications language, application software, Application Software Installation Server
Next: Applications Programming Interface, Application Visualisation System